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| EXAMINER | |
|---|---|
| PASIA, REDENTOR M | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/761,395 | BURTON ET AL. | |
| | Examiner | Art Unit | |
| | REDENTOR M. PASIA | 2416 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 14, 2008 has been entered.

### *Response to Amendment*

2. Applicant's amendment filed on October 14, 2008 has been entered. Claim 19 has been amended. No claims have been canceled. Claims 21-23 have been added. Claims 19-23 are still pending in this application, with claims 19 and 23 being independent.

### *Response to Arguments*

3. Applicant's arguments with respect to claims 19-23 have been considered but are moot in view of the new ground(s) of rejection.

### *Specification*

4. The disclosure is objected to because of the following informalities:

Par. 0019 shows "This device also has a transmit cell first in first out (FIFO) circuit adapted to build a packet header based on data received from the micro-engines payload from the

memory controller" (emphasis on the underlined part). This part is a run-on sentence. It is not clear what the passage desires to state. However, the Examiner has interpreted the above-passage as being the same as "This device also has a transmit cell first in first out (FIFO) circuit adapted to build a packet header based on data received from the micro-engines ~~payload from the memory controller~~".

Appropriate correction is required.

### *Claim Objections*

5. Claim 23 is objected to because of the following informalities: Claim 23 shows the limitation "packet date" in line 11. However, it is understood that the limitation meant "packet data". This interpretation has also been applied to the rejection of the claim. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 23 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 23 recites the claim limitation "generating a packet header based on the payload data". The specification shows details (in Par. 0024, 0027) of building/assembling a packet based on header and payload. While it is enabling to build/assemble a packet based on header and payload, it is not enabling to "generating a packet header based on the payload data".

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 19-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 19 shows the claim limitation "packet data" in line 9. It is unclear if "packet data" in line 9 is related to "packet header data" in line 7 since both claim limitations are received from a memory controller. If they are related, "packet data" in line 9 must be revised to "packet header data". However, in the rejection of the claim, the Examiner has interpreted "packet data" in line 9 as being the same as "packet header data" which ultimately refers to the payload of the packet. The same rejection (and interpretation) applies to other occurrences of "packet data" in claim 19.

Claim 19 shows the claim limitation "packet payload" in line 14. It is unclear if "packet payload" in line 14 is related to "packet header data" in line 7. If they are related, "packet payload" in line 14 must be revised to "packet [[payload]] header data". However, in the rejection of the claim, the Examiner has interpreted "packet payload" in line 14 as being the same as "packet header data" which ultimately refers to the payload of the packet.

Claim 19 shows the claim limitation “payload data” in line 14. It is unclear if “payload data” in line 14 is related to “packet header data” in line 7. If they are related, “payload data” in line 14 must be revised to “[[payload]] packet header data". However, in the rejection of the claim, the Examiner has interpreted "payload data" in line 14 as being the same as "packet header data" which ultimately refers to the payload of the packet.

Claim 20 shows the claim limitation “packet header” in line 19. It is unclear if “packet header” in line 19 is related to “header data” in line 6 since both claim limitations are received from the micro-engine. If they are related, “packet header” in line 19 must be revised to “[[packet]] header data". However, in the rejection of the claim, the Examiner has interpreted “packet header” in line 19 as being the same as "header data" which ultimately refers to the header of the packet.

Claim 20 shows the claim limitation “packet payload” in line 20. It is unclear if “packet payload” in line 20 is related to “packet header data” in line 7 since both claim limitations are received from a memory controller. If they are related, “packet payload” in line 20 must be revised to “packet [[payload]] header data". However, in the rejection of the claim, the Examiner has interpreted “packet payload” in line 20 as being the same as "packet header data" which ultimately refers to the payload of the packet.

Claim 23 shows the claim limitations “packet data” in line 10, “packet payload” in line 14 and “payload data” in line 15. However, based from the specification in Par. 0024, 0027, the above-mentioned claim limitations refer to “payload data". Still, claim language presented is not clear whether each of the limitations are related to each other.

In the examination of the claims, the Examiner has interpreted the above-mentioned claim limitations are being the same as "payload data".

### *Claim Rejections - 35 USC § 103*

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 19-20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lincoln et al. (US 6,829,240; hereinafter Lincoln) in view of Leger et al. (US 5,771,356; hereinafter Leger.).

**As to claim 19**, Lincoln shows a device (device shown in Figure 2 performing the flowchart shown in Figures 3-4; claim 1 of Lincoln) comprising:

first circuitry (Note the main circuitry disclosing all the components shown in Figure 2) to generate a packet (col. 4, lines 41-54; note that the function of the segmentation state machine 50 is to combine the header and payload to create a "recombined cell".) based on header data received from a micro-engine (col. 4, lines 18-54; note that header is introduced by the control memory 38 to the segmentation state machine) and packet header data from a memory controller (col. 4, lines 18-54; note that the segmentation state machine 50 combines the header and the payload in the transmit FIFO 48; however, prior to this step, segmentation state machine reads addresses from the control memory 38 that indicated where cell payloads are stored in host memory 32 (claimed memory controller).), the first circuitry comprising:

second circuitry (Figure 2, segmentation state machine 50) to receive packet data from the memory controller (col. 4, lines 18-54; segmentation state machine reads addresses from the control memory 38 that indicates where cell payloads are stored in host memory 32 (claimed memory controller).) and

to store the packet data in first-in first-out (FIFO) circuitry (col. 4, lines 18-54; the addresses are applied by the segmentation state machine 50 to segmentation DMA 46 to direct the cell payloads to the transmit FIFO 48.); and

third circuitry (Figure 5, TX FIFO) to track a start lane in the FIFO circuitry, and to determine a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO circuitry (Figure 6; col. 9, lines 10-20; col. 7, lines 45-63; both the host transmit FIFO 150 and the host receive FIFO 154 should insure that they maintain cell alignment. The host transmit FIFO 150 maintains cell alignment by transferring a cell payload only when there is at least one (1) complete cell (or any specified number of cells other than one

(1)) at the start of a transfer from the address in the FIFO. The FIFO address 193 in the control memory 38 corresponding to the ATM header is then read from the control memory 38 as indicated at 194 in FIG. 6. This indicates where, in host memory space for the host transmit FIFO 150, the payload for the cell (identified by the ATM header read at 190) is located.).

Even though, Lincoln shows a start lane in the FIFO circuitry (as discussed above), Lincoln does not specifically show, that the start lane indicates a start of free space in the FIFO circuitry.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Leger. Leger shows an invention that relates generally to peripheral hardware controllers in computer systems, and more particularly to any controller that uses a FIFO to control input/output (I/O) data transfer across a CPU bus to and from peripheral devices (col. 1, lines 7-11).

Specifically, Leger shows the start lane indicates a start of free space in a FIFO (Figure 6 shows a generic FIFO controller; col. 6, lines 39-59; note that the FIFO level calculator 603 determines the FIFO_level. The FIFO_level can be expressed in terms of empty (free) space.).

In view of the above, having the system of Lincoln then given the well-established teaching of Leger, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Lincoln as taught by Leger in order to provide better bus load balance and hence more efficient bus utilization (col. 2, lines 22-25).

**As to claim 20**, modified Lincoln shows logic (Lincoln: Figure 3-4, 6) to synchronize receipt of the packet header from the micro-engine and the packet payload from the memory controller (Lincoln: col. 7, lines 45-63; the ATM header 189 is read from the control memory 38

as indicated at 190. This is the header that was previously provided as at 110 in FIG. 4. This header is transferred as at 192. The FIFO address 193 in the control memory 38 corresponding to the ATM header is then read from the control memory 38 as indicated at 194 in FIG. 6. This indicates where, in host memory space for the host transmit FIFO 150, the payload for the cell (identified by the ATM header read at 190) is located. Note that synchronization was performed in the above manner.)

to store the packet header in the FIFO circuitry (Lincoln: col. 6, lines 22-25; The header value and the protocol information in the VCC 2 block are read from the control memory 38 as indicated at 108 and 109 respectively in FIG. 4. The header value is then transferred to the transmit FIFO 48 in FIG. 2 as indicated at 110 in FIG. 4), and

to transfer the packet header and packet payload data from the FIFO circuitry (Lincoln: Figure 2; col. 4, lines 42-54; the recombined cell (header and the payload) is passed to the transmit cell interface line 45) to a destination specified in the packet header (Lincoln: col. 4, lines 4-17; The header indicates the path which is being followed to pass the cells to a central office 22 and toward a desired destination.).

**As to claim 23**, Lincoln shows a method (Figures 3-4, 6-7) comprising:

receiving packet data from a memory controller (col. 4, lines 18-54; segmentation state machine reads addresses from the control memory 38 that indicated where cell payloads are stored in host memory 32 (claimed memory controller).);

storing the packet data in first-in first-out (FIFO) queue (col. 4, lines 18-54; the addresses are applied by the segmentation state machine 50 to segmentation DMA 46 to direct the cell payloads to the transmit FIFO 48.);

tracking a start lane in the FIFO queue and determining a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO queue (Figure 6; col. 9, lines 10-20; col. 7, lines 45-63; both the host transmit FIFO 150 and the host receive FIFO 154 should insure that they maintain cell alignment. The host transmit FIFO 150 maintains cell alignment by transferring a cell payload only when there is at least one (1) complete cell (or any specified number of cells other than one (1)) at the start of a transfer from the address in the FIFO. The FIFO address 193 in the control memory 38 corresponding to the ATM header is then read from the control memory 38 as indicated at 194 in FIG. 6. This indicates where, in host memory space for the host transmit FIFO 150, the payload for the cell (identified by the ATM header read at 190) is located.); and

generating a packet header based on the payload data (col. 4, lines 41-54; note that the function of the segmentation state machine 50 is to combine the header and payload to create a "recombined cell".).

Even though, Lincoln shows a start lane in the FIFO circuitry (as discussed above), Lincoln does not specifically show, that the start lane indicates a start of free space in the FIFO queue.

Specifically, Leger shows the start lane indicates a start of free space in a FIFO (Figure 6 shows a generic FIFO controller; col. 6, lines 39-59; note that the FIFO level calculator 603 determines the FIFO_level. The FIFO_level can be expressed in terms of empty (free) space.).

In view of the above, having the system of Lincoln then given the well-established teaching of Leger, it would have been obvious to one of ordinary skill in the art at the time of the

invention to modify the system of Lincoln as taught by Leger in order to provide better bus load balance and hence more efficient bus utilization (col. 2, lines 22-25).

13. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lincoln et al. (US 6,829,240; hereinafter Lincoln) in view of Leger et al. (US 5,771,356; hereinafter Leger.) in further view of An et al. (US 6,061,361; hereinafter An).

**As to claim 21**, (modified Lincoln shows the micro-engine (as discussed above), however, modified Lincoln does not specifically show that the micro engine is a direct memory access (DMA) controller send queue to transmit requests and receive responses.

However, the above-mentioned claim limitations are well-established in the art as evidenced by An. Specifically, An shows a direct memory access (DMA) controller send queue (Figure 2; RX DMA Agent 28, 32) to transmit requests and receive responses (Figure 3; col. 3, lines 33 to 67; RX DMA agent sends a request signal and waits for a grant signal (claimed response).).

In view of the above, having the system of modified Lincoln, then given the well-established teaching of An, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Lincoln as taught by An in order to enable the data controller to selectively grant access for a specific activity that may require access to one or more buses, even if multiple requests are received simultaneously (col. 2, lines 7-10).

14. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lincoln et al. (US 6,829,240; hereinafter Lincoln) in view of Leger et al. (US 5,771,356; hereinafter Leger.) in further view of Cherukuri (US 5,878,217; hereinafter Cherukuri).

**As to claim 22**, modified Lincoln shows the micro-engine (as discussed above), however, modified Lincoln does not specifically show that the micro engine is a direct memory access (DMA) controller receive queue to transmit response and receive requests.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Cherukuri. Specifically, Cherukuri shows a direct memory access (DMA) controller receive queue (Figure 2, DMA Controller 206) to transmit response and receive requests (Note that arrows indicate that DMA controller 206 receives DMA requests and transmits DMA acknowledgement (claimed response).).

In view of the above, having the system of modified Lincoln, then given the well-established teaching of Cherukuri, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Lincoln as taught by Cherukuri in order to keep the data in the proper sequence since switching may cause the order of the data to be processed out of its intended sequence (col. 2, lines 36-38).

15. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lincoln et al. (US 6,829,240; hereinafter Lincoln) in view of Leger et al. (US 5,771,356; hereinafter Leger.) in further view of Vogel (US 6,839,352; hereinafter Vogel).

As to claim 23, Lincoln shows a method (Figures 3-4, 6-7) comprising:

receiving packet data from a memory controller (col. 4, lines 18-54; segmentation state machine reads addresses from the control memory 38 that indicated where cell payloads are stored in host memory 32 (claimed memory controller).);

storing the packet data in first-in first-out (FIFO) queue (col. 4, lines 18-54; the addresses are applied by the segmentation state machine 50 to segmentation DMA 46 to direct the cell payloads to the transmit FIFO 48.); and

tracking a start lane in the FIFO queue and determining a starting lane for packet payload such that alignment of payload data matches the start lane in the FIFO queue (Figure 6; col. 9, lines 10-20; col. 7, lines 45-63; both the host transmit FIFO 150 and the host receive FIFO 154 should insure that they maintain cell alignment. The host transmit FIFO 150 maintains cell alignment by transferring a cell payload only when there is at least one (1) complete cell (or any specified number of cells other than one (1)) at the start of a transfer from the address in the FIFO. The FIFO address 193 in the control memory 38 corresponding to the ATM header is then read from the control memory 38 as indicated at 194 in FIG. 6. This indicates where, in host memory space for the host transmit FIFO 150, the payload for the cell (identified by the ATM header read at 190) is located.).

Even though, Lincoln shows a start lane in the FIFO circuitry (as discussed above), Lincoln does not specifically show, that the start lane indicates a start of free space in the FIFO queue and the step of generating a packet header based on the payload data.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Leger. Specifically, Leger shows the start lane indicates a start of free space in a FIFO (Figure 6 shows a generic FIFO controller; col. 6, lines 39-59; note that the FIFO level

calculator 603 determines the FIFO_level. The FIFO_level can be expressed in terms of empty (free) space.).

In view of the above, having the system of Lincoln then given the well-established teaching of Leger, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Lincoln as taught by Leger in order to provide better bus load balance and hence more efficient bus utilization (col. 2, lines 22-25).

Still, modified Lincoln does not specifically show the step of generating a packet header based on the payload data.

However, the above-mentioned claim limitations are well-established in the art as evidenced by Vogel. Specifically, Vogel shows the step of generating a packet header based on the payload data (Figure 3, single-chip SONET physical layer device 30; Figure 4; col. 5, lines 31-42; col. 7, lines 34-48; interface block 42 then generates the header fields 12 for each of the ATM cells 10 based on the header field extracted from the PPP payload field.).

In view of the above, having the system of modified Lincoln then given the well-established teaching of Vogel, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of modified Lincoln as taught by Vogel in order to implement a particular protocol consistent with the application in which a device is used for maximizing transmission bandwidth (col. 3, lines 50-55).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REDENTOR M. PASIA whose telephone number is (571)272-9745. The examiner can normally be reached on M-F 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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